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RELIABLE MINIATURE SPACEBORNE MEMORY

FINAL REPORT

October 1967

Contract No. NAS5-9518

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

Goddard Space Flight Center

Greenbelt, Maryland

UNIVAC

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ABSTRACT

This report presents the final documentation of the breadboard model of a miniature spaceborne memory. The memory system which has been delivered has the following characteristics:

Memory Element	Magnetic, thin film, plated-wire.	
Storage Capacity	1,216,512 bits.	
Speed	500-kilocycle serial bit rate.	
Operating Mode	Nondestructive readout, serially addressed buffer memory.	
Input Voltages	+24.5 volts ±2% - 3.0 volts ±2%	
Power Consumption (excluding converter losses)	Standby: 500-kilocycle writing: 500-cilocycle reading:	0.579 watts 1.60 watts 1.64 watts
Operating Temperature Range	25°C to 60°C.	

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SECTION 1

INTRODUCTION

The objective of this contract was to design a 2.8×10^6-bit Miniature Spaceborne Memory System. This memory was to have two independent memories of 1.4×10^6-bits. A breadboard model of a 1.4×10^6-bit memory has been delivered, and the main object of this report is to document the breadboard model together with a memory exerciser which has been delivered.

The details of the design of the system have been reported in the Interim Engineering Report which was submitted at the conclusion of the design phase. The main object of Section 2 is to present a summary of the significant development and problems encountered during the project. Section 3 presents further background information on the plated wire and gives test procedures and results.

The block diagram and timing diagrams are presented in Section 4 together with the detailed input-output specifications.

The packaging of the breadboard model and memory exerciser is shown in Section 5.

The component selection and the design derating rules are given in Section 6. The circuit design reports were given in the Interim Engineering Report and the circuit schematics are included in Appendix I. Section 7 gives the results of system test.

The detailed logic and circuit drawings are given in Appendix I together with all information necessary for their understanding.

The main mechanical drawings for the memory stack, which has been packaged in its final form, are given in Appendix II. The details of the design of the stack were presented in the Interim Engineering Report.

The operating instructions and logic drawings for the Memory Exerciser are given in Appendix III.

SECTION 2

PROJECT BACKGROUND

2.1. STATE OF DEVELOPMENT AT START OF PROJECT

Prior to the commencement of this project, Univac completed and delivered a research model memory system to NASA Goddard Space Flight Center. This buffer memory contained approximately 100,000 bits of magnetic thin film plated wire storage capacity. It operated at a 100,000 bit per second information rate in a non-destructive readout mode. It required 88 milliwatts of standby power plus 94 milliwatts of losses in a d.c. to d.c. converter. The maximum operating power during a continuous 100 KC information write mode was 379 milliwatts plus 167 milliwatts of converter losses.

Design and development of a 2.8 million bit capacity plated wire memory system was begun in November 1964. The design specifies two electrically and mechanically independent half memories of 1.4 million bits. A research model of one of these half memories has been built. The operating speed has been increased by a factor of 5 to 500,000 bits per second. The capacity of the memory has been increased 14.7 to 1 to 1,474,000 bits. The operating temperature range has been increased from 70°C (-20°C to +50°C) to 100°C (-20°C to +80°C) and the storage temperature was set at +150°C to allow sterilization of the memory. The model must demonstrate that the memory could be packaged in a Nimbus package 6 inches by 4 inches by 13 inches.

The standby power consumption of the memory is approximately 580 milliwatts. The operating power consumption during a continuous 500 KC write operation is approximately 1.6 watts.

2.2. RELATED AREAS OF PAST AND CURRENT DEVELOPMENT

Plated wire memories are used exclusively as the main memory for the new 9000 series of commercial computers. In addition the following are some of the completed contracts which relate to aerospace plated wire memories.

PLATED WIRE NONDESTRUCTIVE READOUT MEMORY PLANE
CONTRACT NO. 318-IL-H-222310

MASSACHUSETTS INSTITUTE OF TECHNOLOGY
INSTRUMENTATION LABORATORY

13,000-bit memory stacks have been delivered for a high-reliability, airborne weapons system. The stack access time is less than 2 microseconds, and the stack withstands severe mechanical shock. The stack will be expandable to twice its capacity. A set of memory electronics is also provided to exercise the stack.

SATELLITE MEMORY - FLIGHT UNITS
CONTRACT NO. N-163-12940(X)

NAVAL AVIONICS FACILITY, INDIANAPOLIS

Two complete, special-purpose, plated-wire memory systems have been built for use in an operational satellite system. These units use one-tenth of the power and require one-half of the volume and weight of the ferrite core predecessor.

SPACECRAFT MEMORY
CONTRACT NO. NAS 5-3171

GODDARD SPACE FLIGHT CENTER (NASA)

A prototype of a 100,000-bit plated-wire spacecraft memory was designed and delivered to NASA. Features of the memory are 100-kilocycle serial-bit operation, NDRO, and 015-watt power dissipation.

MEDIUM-SPEED MASS RANDOM-ACCESS MEMORY - (Feasibility Model)
CONTRACT NO. AF 30(602)3825

ROME AIR DEVELOPMENT CENTER

A feasibility model of a 100-million-bit plated-wire memory is being built. This model will be partially populated and is the second phase of a program to develop a nonmechanical mass memory. One of the primary goals is a manufacturing cost less than 1 cent per bit.

MANUFACTURING TECHNIQUES
CONTRACT NO. AF 33(615)3019

AIR FORCE MATERIALS LABORATORY
WRIGHT-PATTERSON AFB, OHIO

Manufacturing techniques were developed for producing plated wire in great quantity at low cost. The result of the contract is a wire plater capable of producing 60 million bits per year at a density of 22 bits per inch of plated wire.

2.3 PROBLEMS ENCOUNTERED IN PROJECT

The state of the art of plated wire technology has been advanced in every phase during the project. A summary of the significant developments and problems encountered is presented in this section.

2.3.1. PLATED WIRE ELEMENT

At the beginning of the project, plated wires had only been produced in a research laboratory and there had been very limited life data taken. One of the first problems encountered in this phase was that the uniaxial anisotropy of some plated wires was degraded under high temperature, hard field conditions. An investigation showed that an easy field magnetic anneal prevented this degradation and the following procedure was set up:

1. Magnetize the wire by passage of 150 ma direct current.
2. Place on teflon coated trays in oven and purge with 95% argon-5% hydrogen.
3. Raise oven temperature to 150°C and maintain temperature for 12 hours.
4. Reduce temperature to 125°C and maintain temperature for 6 hours with a hard axis, 5 oersted field.

The last step was performed to test for the effectiveness of the easy field anneal. Although some of the wires in the memory were processed in this manner, poor yields were obtained and 100% testing was required. An investigation showed that the magnetic anneal must be performed with current flowing in the plated wire to assure that the uniaxial anisotropy is magnetically annealed into the nickel iron alloy.

During the time the above work was being done, a plated wire manufacturing facility was set up to produce wire for the 9000 series of computers. On-line ovens were included in the platers to perform the easy field magnetic anneal. Using these wires the following procedure was set up:

1. Bend the wire into the hairpin.
2. Perform a hard field anneal at 125°C.
3. Tin the wire.
4. Test the wire for acceptance for the memory.

The wires processed in this manner were initially 100% tested, but it was shortly found that the wires could be tested on a sampling of the batch. A batch of wires consists of several hundred wires made continuously on the same plater. A sample test procedure was set up which assured high yields in the memory stack. The details of this procedure are given in Section 3.2.

Life tests performed on many batchs of plated wires have shown no long term aging. Some wires, however, have developed bad spots. This is attributed to minor substrate flaws such that the local magnetic moments tend to line up with the substrate flaw. Batchs which exhibit this characteristic are rejected during the testing.

2.3.2. CORROSION PROTECTION OF PLATED WIRES

Prior to this project, the plated wires were coated with a polyurethane to prevent possible corrosion. This was a very costly process and investigations were undertaken to eliminate it.

Protective overplating, using tin, gold and rhodium, was tried to protect the magnetic film from corrosion. It was found that the protective coating tends to be damaged by contact with the mercury cups used to make electrical contact with the wires during manufacture. It was also found that a pinhole-free coating was imperative, and that coating sufficiently thick to be free of pinholes reduced the magnetic output of the wires. Damaged or pin-holed coating proved to produce more corrosion in wires than was seen in uncoated wires.

An extensive investigation showed that the plated nickel iron alloy did not need corrosion protection against a high temperature, high humidity atmosphere when the wires are in the memory teflon tunnel material and have been properly cleaned. The last step in the wire manufacturing process is to clean the wires, and the corrosion problem has been solved simply by using careful handling procedures until the wires are installed in the memory planes.

2.3.3. RETURN WIRE

The plated wires in this memory stack are on 15 mil centers. This is half the spacing of the previous memory design. At this close spacing, it is no longer possible to use the unplated beryllium copper return or noise

cancelling wire as part of the sense line circuit. It was necessary to develop a return wire that matched the attenuation and delay characteristics of the plated wire, did not give any signal output, and provided the same magnetic interactions with the adjacent plated wires. This problem has been solved in two possible ways. The first way involves a special plating with different magnetic characteristics from that used for the memory wire. The second involves the use of a regular plated wire and a thin copper wire in one tunnel structure.

The second approach was chosen because of lower cost. The first approach requires a plating approximately five times as thick as the regular plated wire. Such a wire must be plated very slowly to avoid excessive magnetostriction.

2.3.4. HAIRPIN WIRES

It was decided early in the project to develop a technique of bending the wire in the shape of a hairpin, with the two halves of the hairpin being in two different planes. This saves half of the wire connections since the wire is soldered only at one end of a plane. This configuration also forms an excellent strain relief for the wires since the wire is free to move in the tunnels. The difference of thermal coefficients between the plane and the wire thereby cannot cause a strain on the wire as the temperature of the unit is varied. The hairpin is made by bending the wire over a quartz mandrel and heating the bend with a propane-oxygen torch to relieve the internal stresses. The problems of heat sinking the active portion of the wire and preventing oxidation of the heated portion were overcome, and the hairpin lived up to full expectations.

2.3.5. ELEVEN FOOT SENSE LINE

Tests performed during the design phase showed that the originally contemplated full-turn word drive line was not really suitable for use on a memory with a sense line 11 feet long. The first plated wire memory developed for the Goddard Space Flight Center used these word drive lines but had a sense line which was only two feet long. The work on this project showed the benefits and problems with word drive lines consisting of two complete turns, one complete turn, and one-half turn. The one-half turn drive line provided suitable transmission characteristics for the sense line, but by

itself permitted so much spreading of the word drive field to adjacent bits that it would have been necessary to substantially reduce the bit density along the plated wire. The development of the one-half turn word line then was contingent upon the development of a technique for using a magnetic keeper with each drive line. This magnetic keeper reduces the amount of drive current which would otherwise be required, and permits the highest bit packing density that we have yet achieved. The result has been a substantially simplified construction of the word drive lines and memory plane, a high bit packing density, a reasonable level of drive current operation, and a high signal to noise ratio.

2.3.6. BIT DENSITY

The overall bit packing density of the 1.5 million bit stack that has been designed is approximately 10,000 bits per cubic inch. This figure includes all the necessary connections, diode access matrix for the word line selection, and external case work for the memory stack. This has proved to be one of the most difficult packaging problems because of the stringent requirements upon close tolerance fabrication and assembly of the 12 memory frames that make up the memory stack. A number of items had to be fabricated with the aid of specially designed tools, fixtures, and dies, to permit the achievement of this density. The overall volumetric density is approximately 5 times higher than that of former memory designs.

2.3.7. TUNNEL MATERIAL

One of the severe material problems encountered for the memory stack was that of obtaining the wire carrier material that would meet the tight tolerances necessary for mounting the wires on 15 mil centers. Not only must there be alignment between the tunnel material and the pads to which the wires are soldered, but there must be plane to plane alignment. The solution was obtained only by developing our own in-house capabilities. The tunnel material is fabricated by pressing sheets of teflon and H-film on monel form wires which have been wrapped on a loom with the prescribed tolerances. The teflon flows around the form wires during the pressing, and the form wires are then extracted leaving the 8 mil tunnels.

2.3.8. MATERIAL SELECTION AND TEST

A number of materials used in the fabrication of the memory plane had to be carefully selected and tested to be able to meet the requirement of 150°C storage for 48 hours. Fortunately, suitable materials were found after a significant effort was expended in their selection and subsequent testing. It was found during this investigation that some materials normally considered suitable for 150°C operation proved to be unsuitable when used in the thin sections required by memory plane design. A number of tests and evaluations were performed which showed that aluminum could be substituted by copper in the construction of the memory planes. This was especially significant in this design since it represents a saving of approximately 2 pounds in the 1.5 million bit stack, and the final stack weighs only 9 pounds.

2.3.9. MEMORY STACK INSTABILITY

A mechanical instability when the system was temperature cycled caused a varying alignment between the tunnels which contain the plated wires and the transition bars to which the plated wires are soldered. This resulted in the higher magnetostrictive wires affecting the system operation. The instability is due to different thermal coefficients of expansion of the materials which determine the alignment between the tunnel material and the transition bars. The problem is further aggravated because the transition bar is not rigidly attached to the ground structure such that the transition bar can be at different positions at the same temperature after temperature cycling. This resulted in poor repeatability of error data and a longer period of system test than would normally be required.

The problem was solved in this memory system by replacing the wires which failed during many temperature cycles of the system. Future designs will eliminate the problem by having matched temperature coefficients between the transition bars and the memory frames and by having the transition bars securely attached to the memory frames.

2.3.10. MEMORY STACK EDGE PROBLEMS

Some problems affecting the operation of the plated wires near the edges of a few of the planes forced a reduction in capacity of the memory to 1.21

million bits. A word field nonuniformity exists near the last few word lines in small sections of a few of the planes. This problem would be resolved in future designs without loss of bit density by more careful fabrication procedures to maintain dimensional uniformity and by having dummy word lines at the edge of the planes. A second problem at the B-switch edge of the planes was an interaction in some planes between the word current and the operation of the plated wires. This interaction is caused by the word current flowing parallel to the plated wires in the bus structures which connects the selected A-switch to the selected B-switch. An analysis of this problem is required, but it appears that it can be eliminated without loss of bit density since it did not exist in all planes.

2.3.11. SYSTEM DESIGN

A significant amount of effort was made to obtain an optimum system design. The important parameters that were optimized are:

1. Low power consumption; standby power being somewhat more important than operating power.

2. Minimum number of circuits consistent with reliable operation.

3. Minimum number of internal connections within the 1.5 million bit memory stack. There are 60 bits per connection when all connections are counted including the diode word selection matrix, the bit-sense low level switch matrix, the sense amplifier input cables, the word selection A switches and B switches and the cables to the circuits outside of the stack. This figure could have been substantially improved if it had not been necessary to use the 6 inch by 4 inch by 13 inch box for the memory.

2.3.12. CIRCUIT DESIGN

Several circuit designs very similar to what had been previously designed had to be improved significantly for this 1.5 million bit memory design. In addition to the circuit improvements, which were primarily related to increasing the speed by a factor of 5 over the previous designs, it was also necessary to reduce these designs to a hybrid thin film circuit or hybrid cermet form. This was necessary since it was a requirement of the contract to show conclusively that the memory design could be packaged to fit into a 6 inch by 8 inch by 13 inch volume. To be able to package the entire memory into this volume requires that a miniature form of circuitry be used. The hybrid form was chosen because it permitted the necessary circuit packing

density and operated at lower power than comparable monolithic integrated circuits would have required.

To summarize, a memory system has been designed with a storage capacity of 1.5 million bits, an operating speed of 500,000 bits per second, and a power consumption of 1.5 watts. This represents a speed increase of 5 to 1 and a capacity increase of 28 when compared to the previous memory design. The total power consumption has increased approximately 3 to 1. In addition to the performance and storage capacity advantages, the overall packing density including all circuits for the complete system and external case has reached approximately 5000 bits/cubic inch.

SECTION 3

THE PLATED-WIRE MEMORY ELEMENT

3.1 THEORY OF OPERATION

The memory element consists of a wire substrate which is made of beryllium-copper drawn to a 0.005-inch diameter and which is electroplated with a magnetic thin film. The magnetic film is the same 81 percent nickel, 19 percent iron alloy widely used in planar thin-film memory elements. The coating is continuous and is plated in the presence of a circumferential magnetic field that establishes a magnetic anisotropy axis, or preferred magnetization direction, circumferentially around the wire. Figure 1 is a simplified diagram of the plating apparatus and the electrical test that provides immediate control of the process. The magnetic material is electroplated on a continuously moving wire in room environment. The continuously moving wire is electrically tested with a complete operating memory pulse program.

Information is stored according to the sense of the circumferential magnetization in the portion of the plated wire encircled by the word strap: clockwise magnetization represents a stored 1; counterclockwise magnetization represents a stored 0. Figure 2 shows a sketch of the plated wire and the word drive line which forms a one-turn solenoid. To read the stored information, a word current is applied to the word strap which encircles the plated wire at right angles. The word current produces a word field along the axis of the wire. This word field tilts the magnetization vector from its circumferential rest position towards the axis of the wire. The resulting flux change causes a voltage change (sensed at the ends of the plated wire) of one polarity for a stored 1, and of the opposite polarity for a stored 0. Figure 3 shows a qualitative vector diagram of the magnetization vector position. The amplitude of the word current is controlled so

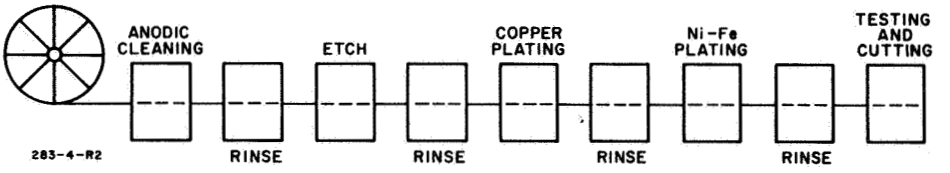


Figure 1. Simplified Diagram of Wire-Plating Apparatus

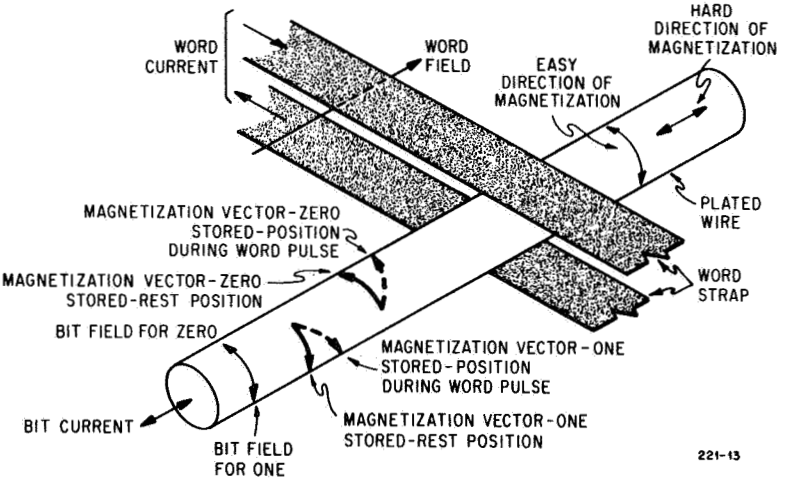


Figure 2. Information Storage on Plated Wire

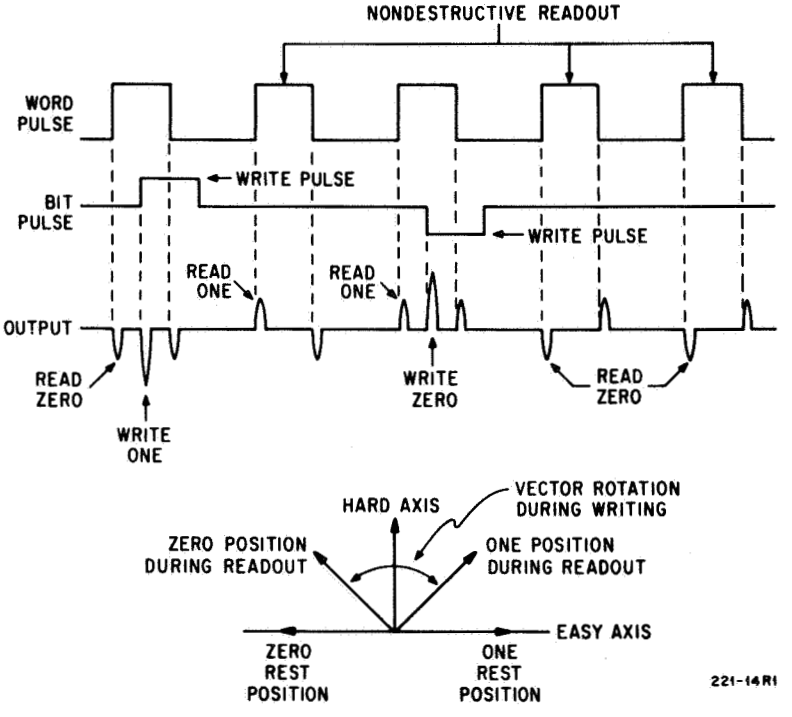


Figure 3. Simplified Diagram of Read and Write Cycles

that when the current is turned off the magnetization vector returns to its origianl rest position under the influence of the anisotropy and demagnetizing fields; thus, the readout is nondestructive.

Information is written into the wire by the time coincidence of the word current and a steering bit current through the plated wire. When the bit current flows in one direction, the magnetization vector is so steered that when the bit and word current end the vector is in the 1 rest position; when the bit current flows in the other direction, the magnetization vector is left in the 0 position.

Operating parameters of the plated wire in the Miniature Spaceborne Memory are as follows:

Word-strap width:	33 mils, 1/2 turn,
Word current:	940 milliamperes writing 900 milliamperes reading
Bit current:	36 milliamperes
Output Flux:	130 millivolt-nanoseconds worst-case with off-nominal currents

The read word current is lower than the write word current to give more stable NDRO operation.

The magnetic plating is continuous and if more than 20 to 25 bits per inch along the wire are used there is a tendency for them to interfere with each other. This interference is reversible. If 0 is written millions of times on each side of a 1 with the program shown in Figure 3 the signal read from the 1 will be diminished. If 1 is written on each side of the center test bit, the signal read from the test bit will be increased. This effect is nearly eliminated by the use of the phase modulated writing technique . This method of writing depends upon the reversibility of the adjacent-bit interference. It eliminates this interference by always writing an equal number of 1's and 0's independent of the stored information. It also eliminates any magnetic history effect. Most magnetic storage elements exhibit a sensitivity to the polarity of the information stored in the preceding write operations. Phase modulated writing means that every storage location experiences equal numbers of 1's and 0's in the preceding write operations. This is accomplished during a write operation by first writing the opposite information and then the desired information to be written.

3.2. TEST PROCEDURE

One of the significant developments during the contract was establishing a test procedure for the plated wires which would assure high yields in the stack. A history of this development is given in Heading 2.3.1. The details of the final procedure are given here. Although the wires are continuously tested with a complete memory program as they are made, the manufacturing testing is only performed to guarantee room temperature operation. Additional testing is therefore required to assure a high yield in the stack through the temperature range. It has not been attempted to set up a testing program which would guarantee a 100% yield in the stack since this would cost more than the replacement of a small percentage of the wires after their installation.

The additional testing of the wires was done in a plane identical to the memory planes using mercury cup contacts. The batches of wires were tested on a one out of twenty batch sampling basis, with a minimum sample of five wires. If more than one bit failed during the testing, the batch was rejected. The sample wires were tested for all worst case patterns at four settings of word and bit currents. The test points, together with a plot of the memory operating area, is shown in Figure 4. The following breakdown summarizes the test conditions:

Test	I_B(MA)	I_W(MA)	Flux (MV-NS)
1	35	<590	60
2	<22	825	60
3	>50	790	60
4	35	850	>140

The test conditions were arrived at by correlating wire characteristics with operating results in the memory. Tests 1 and 2 guarantee a low threshold to write characteristic. Test 3 guarantees a high bit disturb threshold such that the magnetization is not changed by bit current alone. Test 4 guarantees a high NDRO characteristic such that the magnetization is not changed by word current alone.

In Test 1, I_W is measured; in Tests 2 and 3 I_B is measured; in Test 4 the flux output is measured. These measurements are performed both before and after the wires are subjected to a 5 oersted hard field for 1 hour at

125°C. This is done to reject batchs which will develop bad spots during high temperature operation.

The sample testing is done only at room temperature. The tests that are performed, however, guarantee that the wires will operate in the stack through the temperature range. First, the wires are tested to wider margins than are required to allow for degradation of performance when they are soldered down. This is necessary since the wires will be somewhat stressed when they are soldered. Secondly, it was found that the wires which did not operate through the temperature range (-5°C to 60°C) in the system did not operate at low bit currents at room temperature. Apparently the films of these wires were stressed when plated and the stress was increased at either the low or high temperature because of the difference in thermal coefficients of expansion between the film and the substrate such that the wires did not operate with adequate margins through the temperature range. The wires which operated below 22 milliamperes at room temperature, however, operated without difficulty through the temperature range.

3.3 TEST RESULTS

The use of the test procedure outlined in Heading 3.2 gave very good results in the memory stack. Well over 95% of the wires installed which passed the test procedure operated satisfactorily. The shmoo shown in Figure 4 is the operating shmoo of the memory stack at room temperature. The operating word currents in Figure 4 are 30% lower than those in Figure 21 because the wires in the memory are on 15 mil centers and operate at 30% higher word current than in the test plane.

Althrough the system was completed to operate only between 25°C and 60°C, an investigation indicated that replacing the wires which did not operate at the low temperature would allow operation over the full temperature range.

It should be emphasized that the wires generally operated as well in the memory as in the wire test. The testing of the wires was done to guarantee a high yield of installed wires, whereas the testing of the system was done to guarantee an adequate operating range.

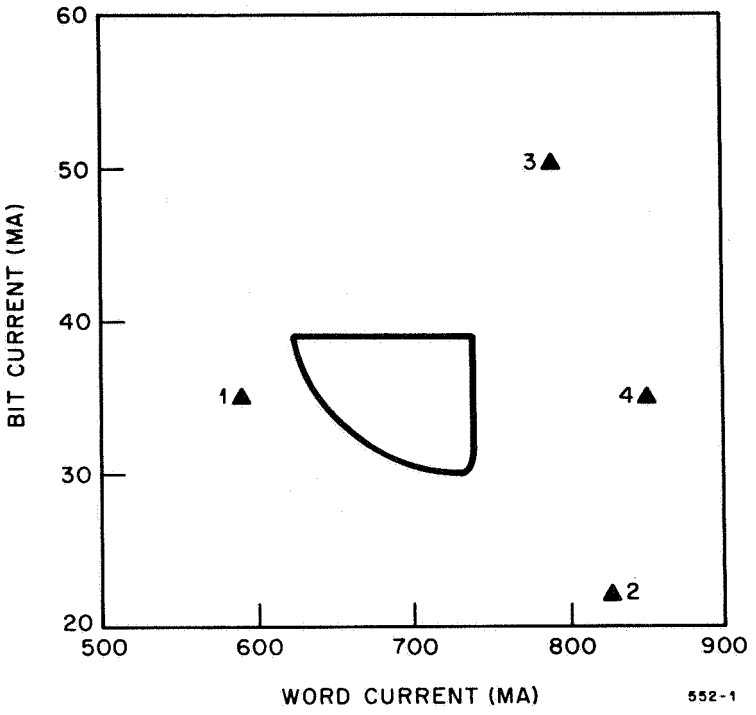


Figure 4. Wire Operating Characteristics and Test Points

SECTION 4

MEMORY SYSTEM ORGANIZATION

4.1. INPUT-OUTPUT SPECIFICATIONS

The input signals, as specified in the contract schedule, have levels of 0±0.5 volt and plus (+) 2.5 ±0.5 volts, have source impedances up to 5000 ohms, and have maximum rise and fall times of 0.5 microseconds. The memory is controlled by three input signals, whose functions and individual requirements are as follows:

1. Input Clock

   The controlling clock for the memory, as specified in the contract schedule, is the negative going edge of a square wave. The memory accepts periodic or non-periodic clock signals at any rate up to 500 KC. During a read operation, one bit of information is transferred to the Output Data line (Signal 4) when the negative going edge of the input clock occurs. During the write operation, one bit of information is transferred to the memory from the Input Data line (Signal 3) when the negative going edge of the input clock occurs. It is not necessary that the input clock be a square wave. The memory will operate with a 1.0 μs negative input pulse.

2. Read-Write Command

   This signal determines whether information is being transferred into or out of the memory. The read command is the high level (+2.5 V), and the write command is the low level. When the signal changes from the read command to the write command (negative going), the memory is ready to accept the first bit of information. When the signal changes from the write command to the read command, there is a maximum delay of 120 microseconds, during which time no output data is available. The presence of the first bit of information on the Output Data line (Signal 4) is given by the Output Clock (Signal 5) which is developed from the Input Clock. No Output Clock will occur during the delay time if Input Clocks are applied.

   The change of state of the Read-Write command is used to clear the memory counters. If during a read operation it is decided to start the operation over, a negative pulse greater than 1.0

microsecond in width will clear the memory to its initial condition, and the first bit will be available after the 120 microsecond delay period. If a write operation is to be interrupted, a positive pulse greater than 120 microseconds will clear the memory, and the memory will accept the first bit of information after the pulse goes low. After power to the memory has been turned on, the Read-Write Command must be used to clear the memory.

3. Input Data

This signal is used during a write operation to determine whether a "1" or a "0" is to be written into the memory. A "1" is represented by the high level (+2.5 volts) and the "0" by the low level.

The output signals have levels plus (+) 2.8 ±0.2 volts and 0.2 ±0.2 volts and have maximum rise and fall times of 20 nanoseconds with a 100 picofarad load. The outputs will supply 1.2 milliamperes in the high state and can draw 1.2 milliamperes in the low state. There are four output signals, whose functions and individual characteristics are as follows:

4. Output Clock

This is the readout clock pulse whose negative going edge is required to be coincident with the leading edge of each bit of output information. The width of this negative pulse is 1.0 microsecond. The negative edge of the output clock occurs within 100 nanoseconds after the start of the change of Output Data.

5. Output Data

The readout data is serial NRZ bits as required. The output data switches within 550 nanoseconds after the start of the negative going edge of the Input Clock.

6. End of Write

This signal indicates that all locations in the memory have been written. The signal is a negative 10 microsecond pulse. The leading edge of the signal occurs within 1.6 microseconds after the start of the negative going edge of the Input Clock that transfers the last bit to the memory.

7. End of Read

This signal indicates that the last bit in the memory has been read. The signal is a negative 10 microsecond pulse. The leading edge of the signal occurs within 0.85 microseconds after the start of the negative going edge of the Input Clock that transfers the last bit to the Output Data Line.

There are several restrictions on the time relationship of the input signals. These are as follows:

1. The start of the write command must precede by 900 nanoseconds the start of the negative going edge of the Input Clock which will transfer the first bit to the memory.

2. The start of the write command cannot occur until 1.3 microseconds after the start of the negative going edge of the Input Clock which transfers the last bit out of the memory. If the read operation is interrupted before the entire memory is read, the start of the write command cannot occur until 7.0 microseconds after the start of the last Input Clock.

3. The start of the read command must precede by 400 nanoseconds the start of the negative going edge of an Input Clock.

4. The start of the read command cannot occur until 3.25 microseconds after the start of the negative going edge of the last Input Clock in the write operation.

5. The start of the change of Input Data must precede by 400 nanoseconds the start of the negative going edge of the Input Clock which will transfer the bit of the memory.

6. The Input Data being transferred to the memory by an Input Clock cannot start to change until 500 nanoseconds after the start of the negative going edge of that Input Clock.

It should be noted that before the serial input data is stored in the memory, it is converted to 36 parallel bits. The transfer of the 36 bits to the memory stack occurs after the thirty-sixth clock pulse (or an integral number thereof). Therefore, if the write operation is stopped before the memory is filled, as many as 35 of the last bits could be lost unless a series of false Input Clocks are applied before the Read-Write Command changes.

4.2. BLOCK DIAGRAM AND TIMING

The block diagram of the memory is shown in Figure 5. The detailed logics are given in Appendix I. The functions of the Input-Output signals are given in Heading 4.1. The operation of the memory will be described by describing how information is written into and read out of the system.

4.2.1. WRITING INFORMATION

When an input clock is applied the input data is transferred to the buffer register by timing signal GBRI. See Figure 6 for timing. The

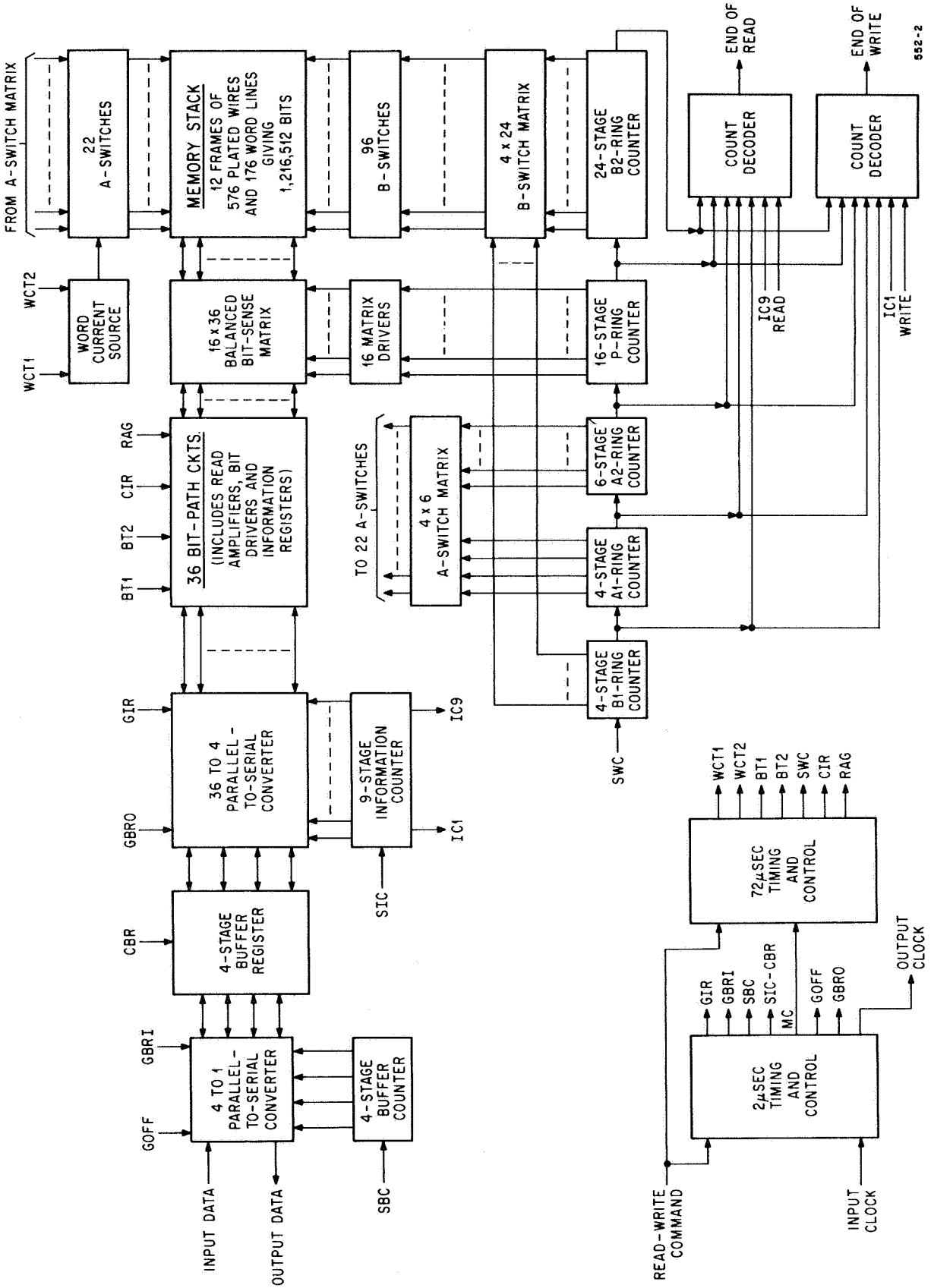


Figure 5. Memory Block Diagram

stage of the buffer register into which the data is transferred is determined by the state of the buffer ring counter. After the input data is transferred to the buffer register, the buffer counter is stepped by timing pulse SBC and the system is ready to accept the next bit of input data. After four bits have been loaded into the buffer register, the four bits are transferred into four of the information registers by timing signal GIR. The four information registers into which the data is transferred are determined by the state of the information ring counter. After the four bits have been transferred, the buffer counter is stepped back to its initial state, the information counter is stepped by timing signal SIC, the buffer register is cleared by timing signal CBR, and the system is ready to accept the next data. After 36 bits of data have been transferred to the memory, the 36 information registers are loaded, the buffer and information counters are stepped back to their initial states, and timing signal MC is generated to initiate the transfer of the information into the memory stack.

When MC occurs, one of 2112 word lines in the memory stack is selected by selecting one of the 22 A-switches and one of the 96 B-switches. The selection of the A-switches is determined by the state of the A1 and A2 ring counters. The selection of the B-switch is similarly determined by the state of the B1 and B2 ring counters. At the end MC, the 36 of 576 plated wire lines into which the information will flow are selected by the bit-sense matrix. The selection of the 36-bit-sense matrix switches is determined by the state of the P ring counter. After the selection of the word and bit swtiches, the 36 bits are written in parallel into the stack using a phase modulated write. The two word currents are controlled by timing pulses WCT1 and WCT2, and the two bit current are controlled by timing pulses BT1 and BT2. See Figure 7 for timing. After the information is written into the stack, the word and bit switches are turned off, the information registers are cleared by CIR, and the information registers are ready to accept incoming information from the buffer registers. The A, B, and P ring counters are then stepped by timing pulse SWC to the next 36 bit address.

The writing process described continues until all 1,216,512 bits have been written and the End of Write signal is generated. Note that continued application of input clocks at this time will start writing the input data into the first locations in the memory.

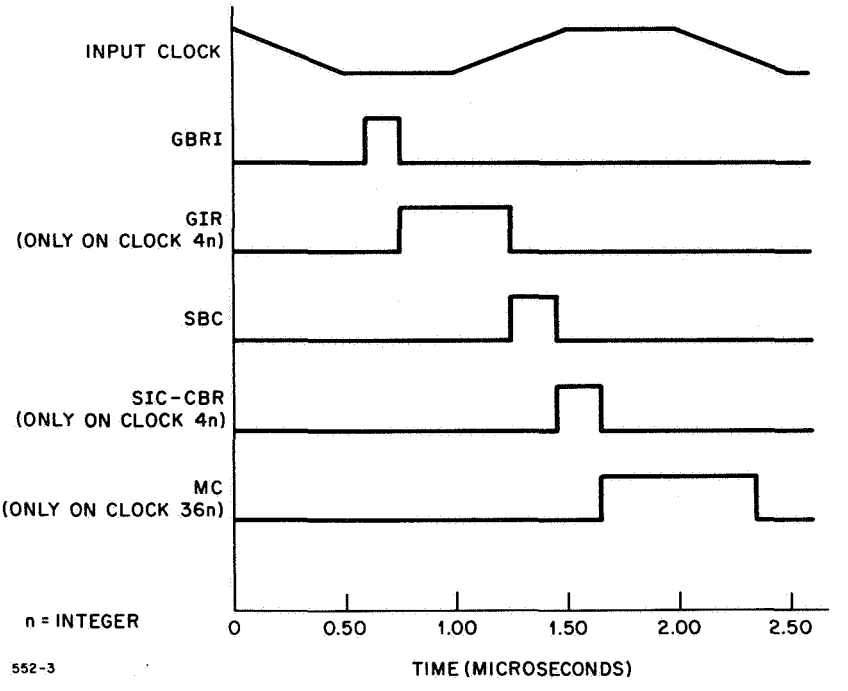


Figure 6. 2μs Write Cycle Timing

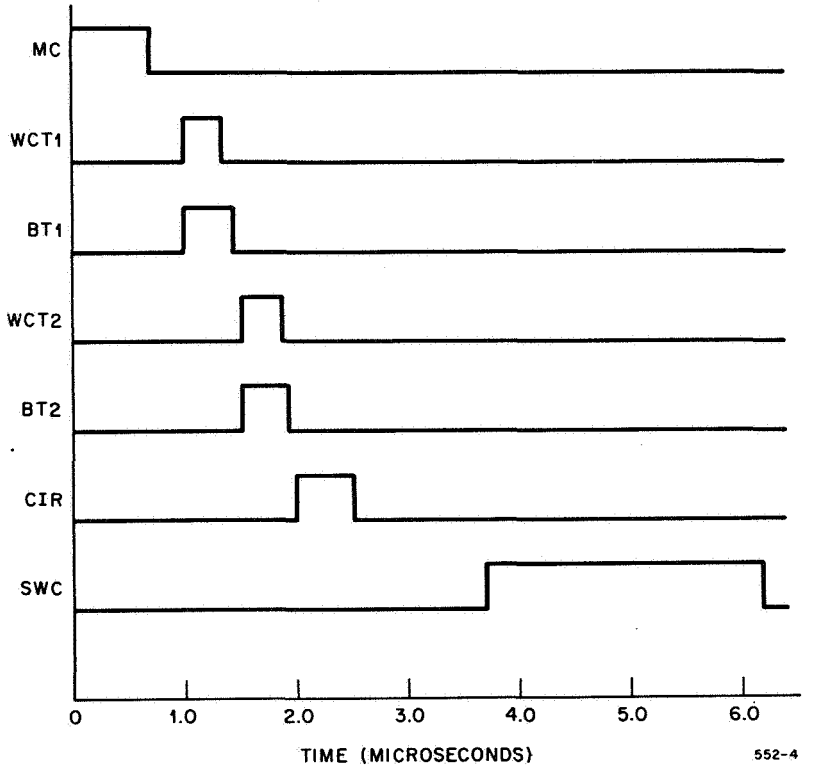


Figure 7. 72μs Write Cycle Timing

4.2.2. READING INFORMATION

Information is read from the memory in the same sequence as it was written. When the read command is given the counters, buffer registers, and information registers are all cleared, the first 36 bits are transferred from the stack to the information registers, the first four bits are transferred from the information registers to the buffer registers, and the B1 counter is stepped to the next 36 bit address. All these functions are performed during the 120 microsecond delay time (heading 4.1) to get the first bit of data ready to be gated onto the output data line.

When the input clock is applied the data is transferred from the buffer register to the output data line by timing pulse GOFF, and the output clock occurs. See Figure 8 for timing. The stage of the buffer register out of which information is transferred is determined by the state of the buffer counter. After the information is transferred to the output data line, the buffer counter is stepped by timing pulse SBC and the system is ready to read out the next bit of data. After four bits have been read out, the buffer counter is stepped back to its initial state, the information counter is stepped by timing pulse SIC, the buffer register is cleared by timing pulse CBR, and the next four bits are transferred from the information register to the buffer register by timing pulse GBRO. The four information registers out of which data is transferred is determined by the state of the information counter. After 32 bits have been read out, and after the 33rd through 36th bits have been transferred to the buffer register, the next 36 bit readout from the memory stack is initiated by timing pulse MC.

When MC occurs, one of 2112 word lines is selected as before, 36 bit-sense matrix switches are selected as before, and the information registers are cleared by timing pulse CIR. See Figure 9 for timing. The 36 bits are read out in parallel by pulsing the word current (controlled by Timing Pulse WCT1) and by gating the read amplifier with Timing Pulse RAG when the plated wire signals caused by the trailing edge of the word current are present at the amplifier. The information is transferred to the information registers by gating the read amplifiers. The A, B, and P ring counters are then stepped to the next 36 bit address by timing pulse SWC.

The reading process described continues until all 1,216,512 bits have been transferred to the output data line and the End of Read signal is

generated. Continued application of input clocks at this point will start reading the information all over again.

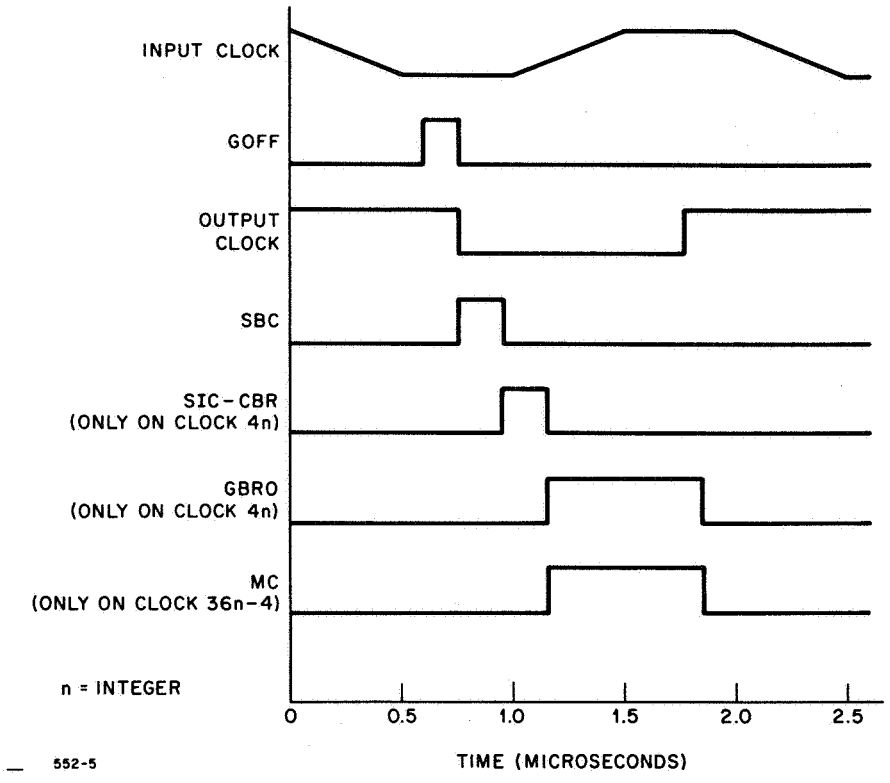


Figure 8. 2μs Read Cycle Timing

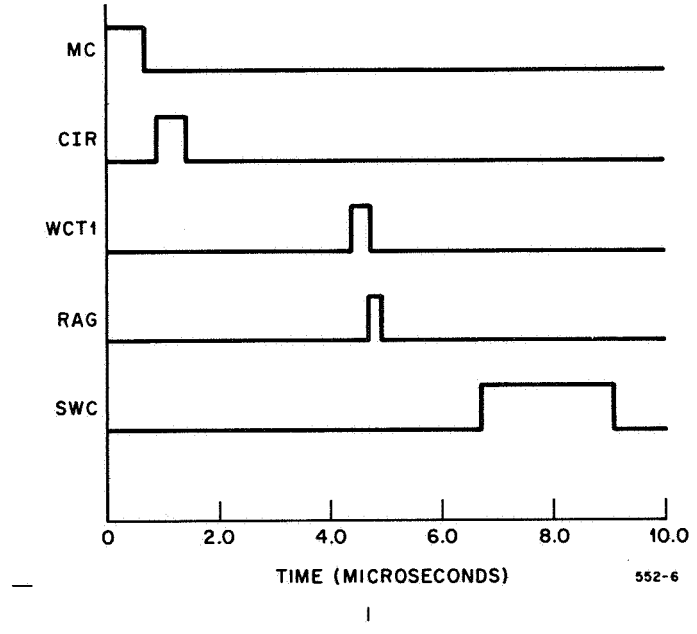


Figure 9. 72μs Read Cycle Timing

SECTION 5

A MEMORY PACKAGING

There was no packaging requirement for the breadboard model. The memory stack, however, was assembled in its final form to demonstrate the feasibility. All materials used in the memory stack were selected to meet the 150°C storage design requirement. The packaging of the rest of the unit was designed in modular form to facilitate convenient testing.

5.1. MEMORY STACK AND BIT-SENSE MATRIX

The memory stack was designed to meet the final requirements of volume, weight, and temperature. The memory stack occupies a volume of 165 cu in. (12 1/4" x 5 3/8" x 2 1/2") and will fit in a standard Nimbus module. The stack weighs approximately 9 pounds, and its required storage temperature of 150°C was demonstrated on a test plane.

A picture of the memory stack and hybrid bit-sense matrix is shown in Figure 10. The packaging of the bit-sense matrix is in its final form except that it is mounted on a heavy brass plate which was necessary to accomodate the connectors. These connectors would not be part of a flight unit, but were incorporated in the breadboard model to facilitate convenient replacement of the plated wires. The A-switch connectors are on the left in Figure 10, the B-switch and bit-sense matrix driver connectors on the right, and the sense line connectors on the top.

A second view of the memory stack is shown in Figure 11. The wiring from the B-switch connector to the B-switch transistors is in the front of the picture, and the 24th memory plane is at the top. Drawings of the memory frame are given in Appendix II.

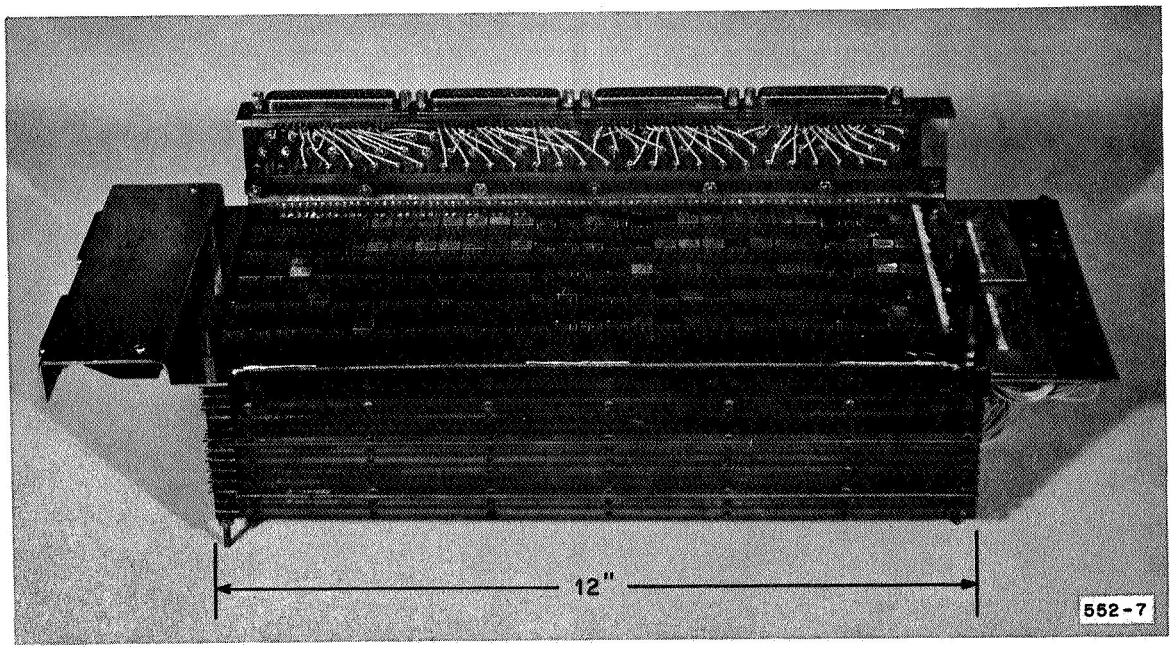


Figure 10. Memory Stack, Connector Plate, and Bit Sense Matrix

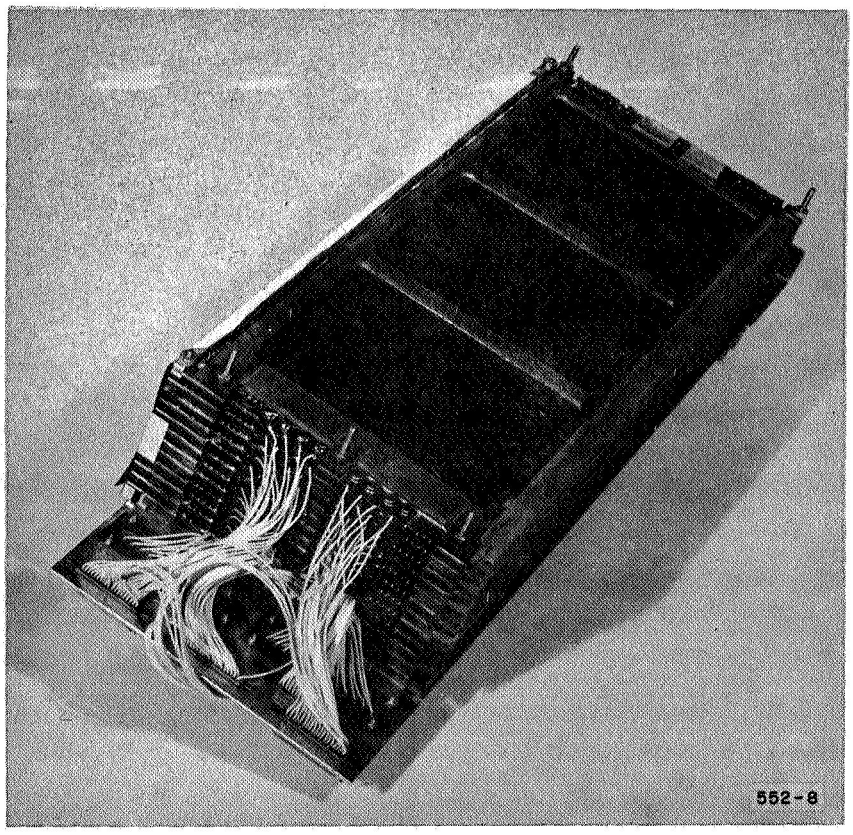


Figure 11. Memory Stack

5.2 PRINTED CIRCUIT CARDS

The electronics packaged with the memory stack includes the bit-sense matrix, switches, word line diodes, and B-switch transistors. The rest of the electronics is packaged on standard double-sided printed circuit cards which plug into wire-wrap connectors. No effect was made to achieve high component densities, since the object was to achieve simple artwork and assembly. The component side of two cards are shown in Figures 12 and 13. The cards are 7" x 5". The connector is on the right, and the card handles, through which contact is made with test points, are on the left. The card in Figure 12 has hybrid circuits made by CTS and transformers made at Univac. The card in Figure 13 has standard components.

5.3. CARD LIBRARY

The test point side of the card library, mounted on the memory chassis, is shown in Figure 14. The cards are mounted on 0.6" centers. The wire-wrap side of the card library is shown in Figure 15 together with the memory stack which is mounted inside its magnetic shield. The B-switch cables going to the memory stack are in the front of the picture.

5.4. INPUT-OUTPUT CONNECTIONS

There are three Cannon type D connectors on the memory cabinet. These are as follows:

Connector	Function	Pin
Voltage	+24.5 volts	1
	- 3.0 volts	8
	Ground	9-15
Exerciser	Pre-wired	-
Input-Output	Read-Write	1
	Input Clock	2
	Input Data	3
	Output Data	4
	Output Clock	5
	End of Write	6
	End of Read	7
	Ground	9-15

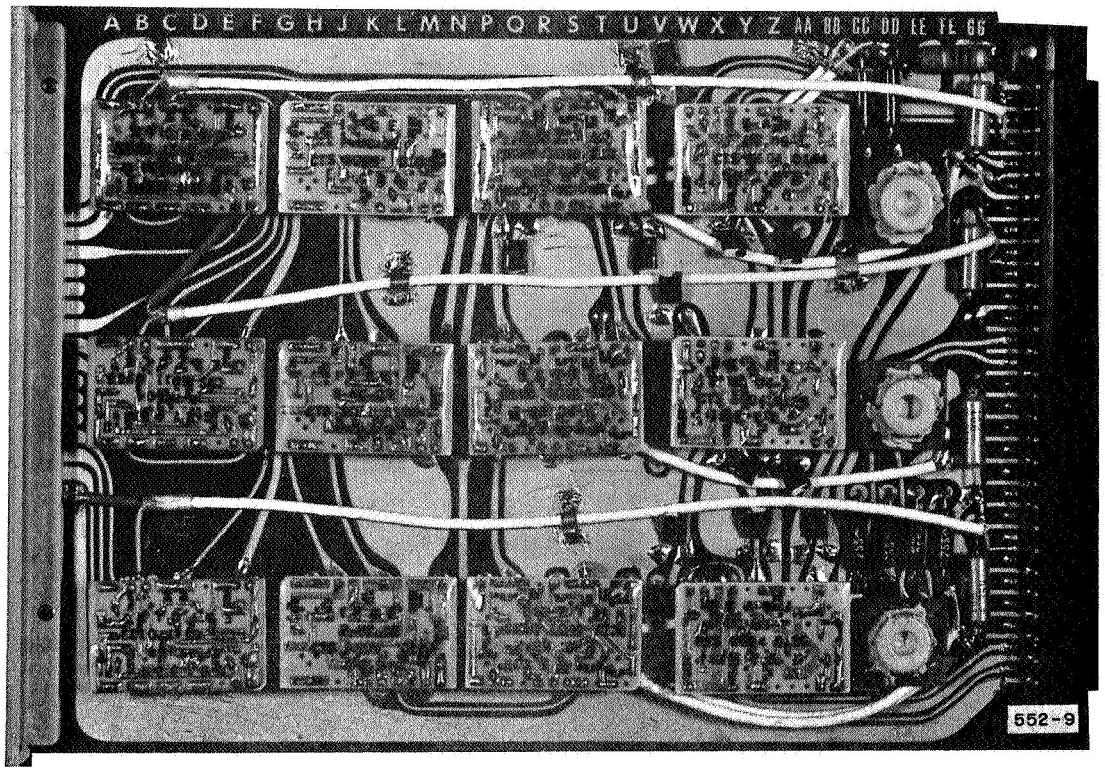


Figure 12. Bit Path Card

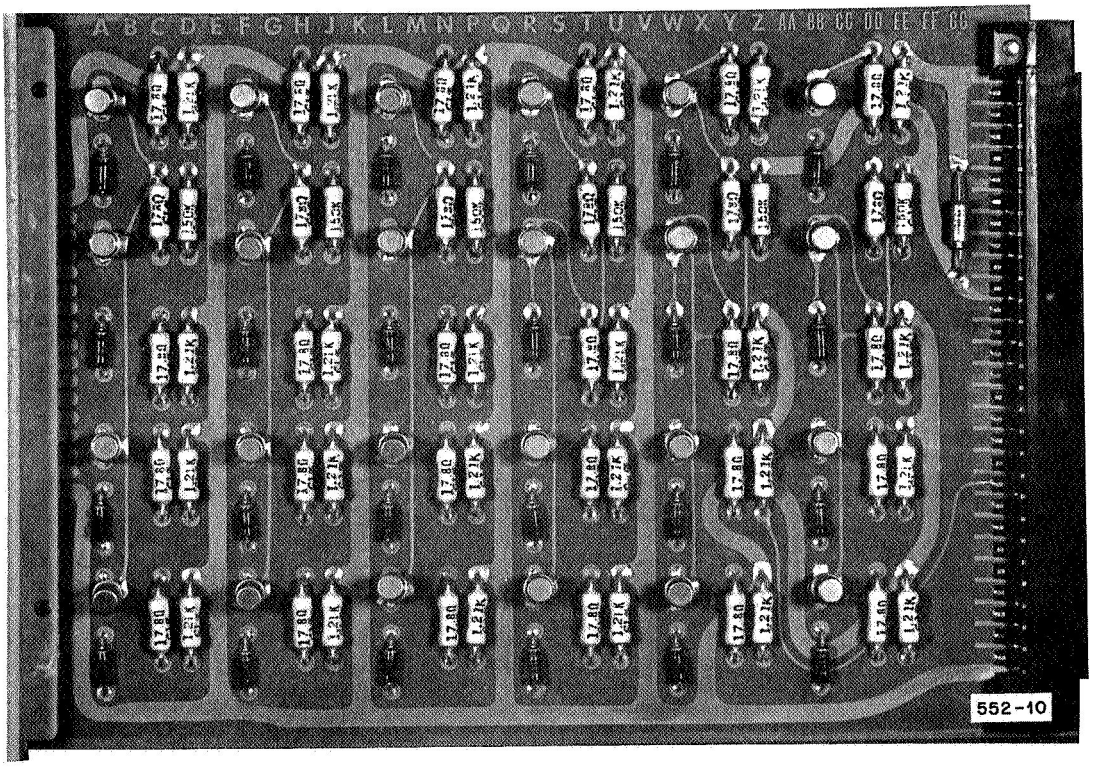


Figure 13. B-Switch Card

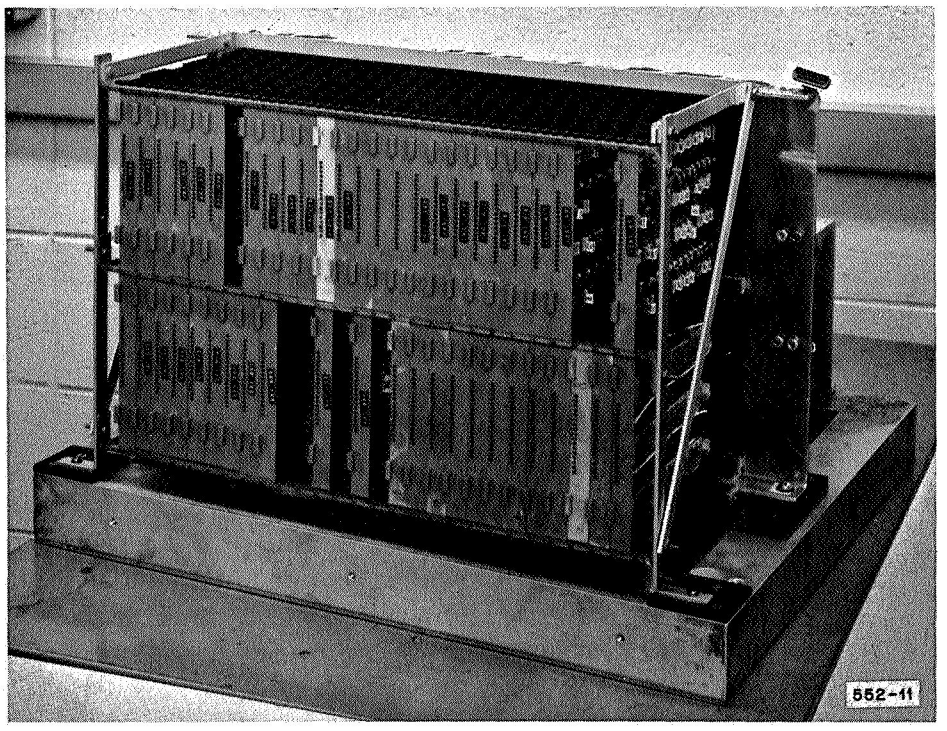


Figure 14. Card Library

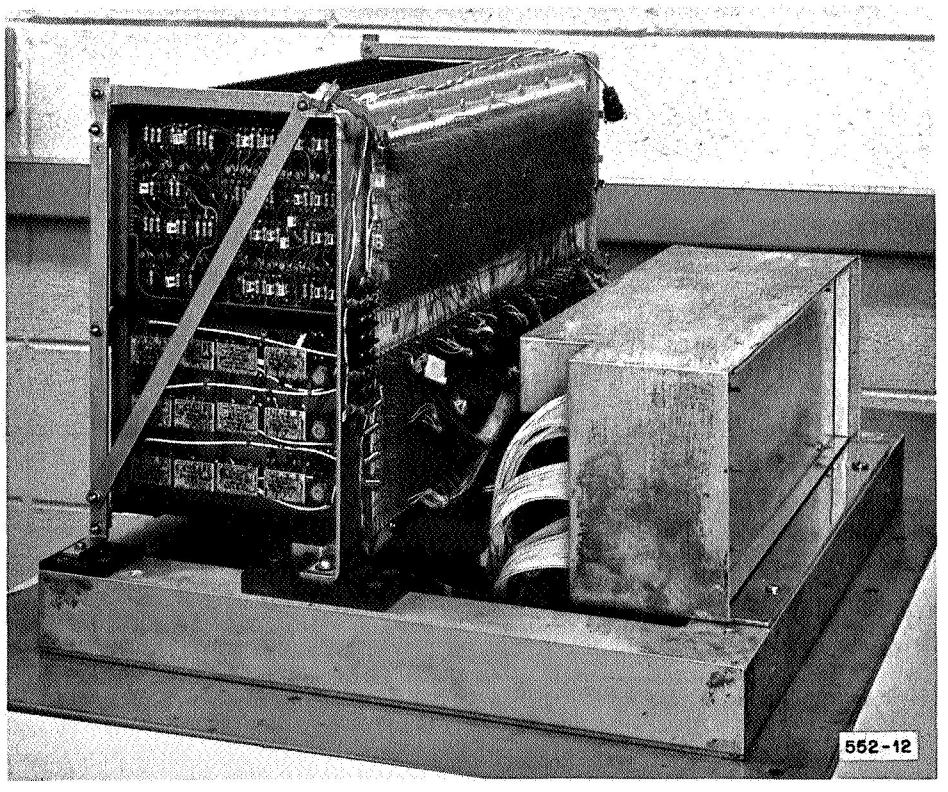


Figure 15. Card Library and Memory Stack

The input-output signals are described in Heading 4-1. When the system is operated with the exerciser, the necessary input-output signals are supplied. If the memory is operated without the exerciser, the exerciser must be disconnected, and similarly, if the memory is operated with the exerciser, the input-output connections should be floating. Either way the memory is operated, the voltages must be supplied. A picture of the memory being operated by the exerciser is shown in Figure 16.

Figure 16. Memory System and Exerciser

SECTION 6

MEMORY CIRCUITRY

6.1. COMPONENT SELECTION

The components selected for the system were electrically identical to those used in the design. Where alternatives in the component selection existed, low cost was the determining factor rather than size. Except for the word line diode modules and hybrid circuits, no pretesting of the components was performed. Although a few components failed during the early stages of system test, no failures occurred during the last three months of the testings.

6.2. DERATING RULES

Worst case design procedures were used throughout the system. In addition to purchase tolerance and temperature coefficients of the components, the following derating factors were used in the design:

Component	Parameter	Derating Factor
Transistor	h_{FE} minimum	0.7
	h_{FE} maximum	1.2
	Breakdown Voltages	0.5
	Leakage Currents	5.0
	V_{BE} maximum	1.1
	V_{BE} minimum	0.9
	V_{CE} maximum	1.2
	C maximum	1.2
	C minimum	0.8

Component	Parameter	Derating Factor
	T_S maximum	1.1
	Total Power	0.5
	Base-Emitter Power	0.1 of total Power
Diode	Leakage current	5.0
	Breakdown Voltage	0.5
	V_F maximum	1.1
	V_F minimum	0.9
	C maximum	1.2
	C minimum	0.8
	T_S maximum	1.2
	V_{Zener}	50 millivolts
	Power	0.5
Resistor	Resistor Value	±2%
Capacitors	Breakdown Voltage	0.5
	Capacitor Value Coupling	±5%
	Bypass	0.5

A further design requirement was that the power supplies could come on in any sequence without damage to any component.

SECTION 7

SYSTEM TEST RESULTS

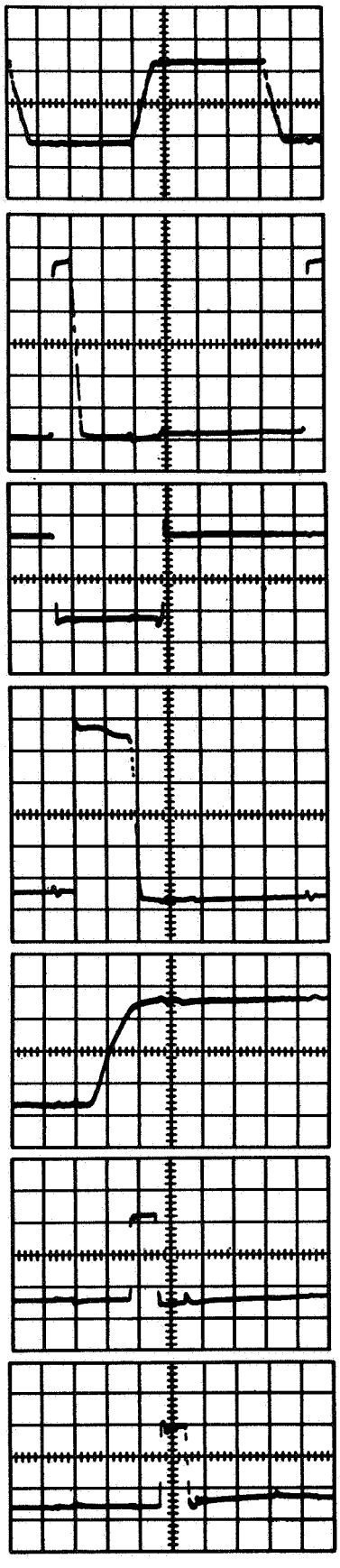
7.1. WAVEFORMS

Figures 17 thru 20 show waveforms described in Section 4.2 and are part of the signals shown in Figures 6 through 9 respectively.

7.2. OPERATING MARGINS

The system was tested at 25°C and 60°C to guarantee stable operation by requiring it to pass two types of tests: (a) system voltage variations to assure adequate margins of the electronics, and (b) word and bit current variations to assure adequate margins in the memory stack.

Although the circuits were designed assuming ±3% supply voltage variations, the system was required to operate with larger variations to take into account component deratings. Accordingly, the system operates with ±20% independent variations of the supply voltages and with all combinations of ±10% variations of the supply voltages. A plot of the operating bit current versus word current is shown in Figure 21. The stack was required to operate to assure error free performance with ±5% tolerances on the nominal bit and word currents. The plot was obtained with a test program consisting of writing the worst case information program and reading the contents of the memory three times. The upper bit current threshold is determined where each storage location received 10,000 bit current disturbs without error. In addition, each storage location was required to withstand 5,000 word current disturbs with the word current 5% above nominal after the worst case information patterns were written with the word and bit currents both 5% below nominal. All these tests were performed with the read amplifier gains varied ±20%. After work on the memory stack was complete, the system was temperature cycled five times between 20°C and 60°C without degradation.



INPUT CLOCK: 1 VOLT/DIV.

GBRI: 2 VOLTS/DIV.

4TH STAGE OF BUFFER REGISTER:
2 VOLTS/DIV.
SHOWS REGISTER BEING SET WITH "1" BY
GBRI AND BEING CLEARED BY SIC-CBR

GIR: 2 VOLTS/DIV.

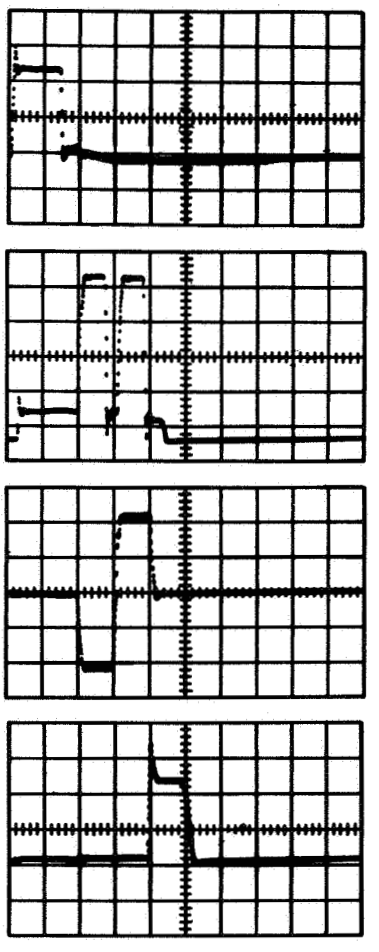
INFORMATION REGISTER BEING
SET WITH "1"
0.5 VOLTS/DIV.

SBC: 2 VOLTS/DIV.

SIC-CBR: 2 VOLTS/DIV.

HOR. SCALE: 250 NS/DIV.

Figure 17. 2μs Write Cycle Waveforms



MC: 2 VOLTS/DIV.

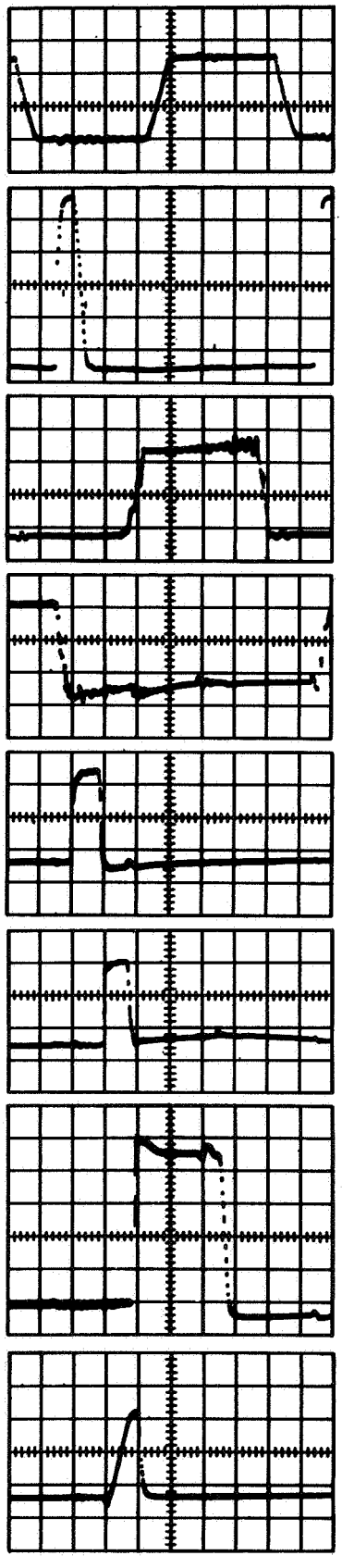
WORD CURRENT: 200 MA/DIV.

BIT CURRENT: 20 MA/DIV.

CIR: 2 VOLTS/DIV.

HOR. SCALE: 500 NS/DIV.

Figure 18. 72μs Write Cycle Waveforms



INPUT CLOCK: 1 VOLT/DIV.

GOFF: 2 VOLTS/DIV.

OUTPUT CLOCK: 1 VOLT/DIV.

NRZ OUTPUT DATA: 1 VOLT/DIV.
SHOWS OUTPUT GOING TO "0" AND
BACK TO "1" ON NEXT CYCLE

SBC: 2 VOLTS/DIV.

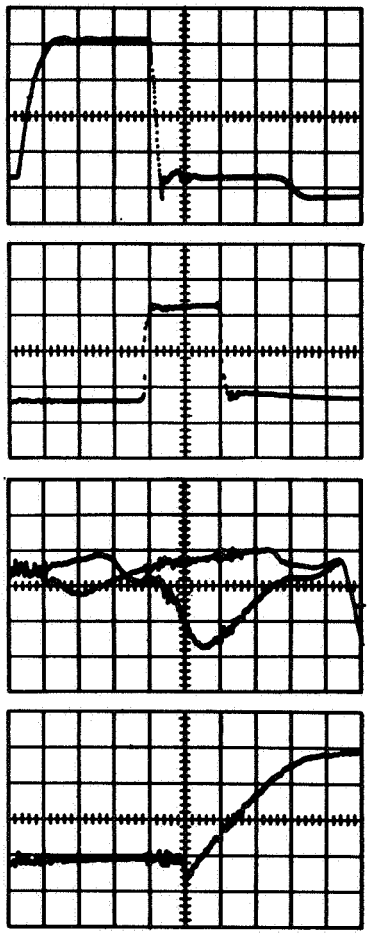
SIC-CBR: 2 VOLTS/DIV.

GBRO: 2 VOLTS/DIV.

1ST STAGE OF BUFFER REGISTER:
2 VOLTS/DIV.
SHOWS REGISTER BEING CLEARED BY
CBR AND THEN BEING SET BY GBRO

HOR. SCALE: 250 NS/DIV.

Figure 19. 2μs Read Cycle Waveforms



WORD CURRENT: 200 MA/DIV.

RAG: 2 VOLTS/DIV.

READ SIGNALS AT DETECTOR STAGE IN AMPLIFIER; "1" IS NEGATIVE TRAILING EDGE SIGNAL. 0.5 VOLTS/DIV.

INFORMATION REGISTER BEING SET WITH "1". 0.5 VOLTS/DIV.

HOR. SCALE: 100 NS/DIV.

Figure 20. 72μs Read Cycle Waveforms

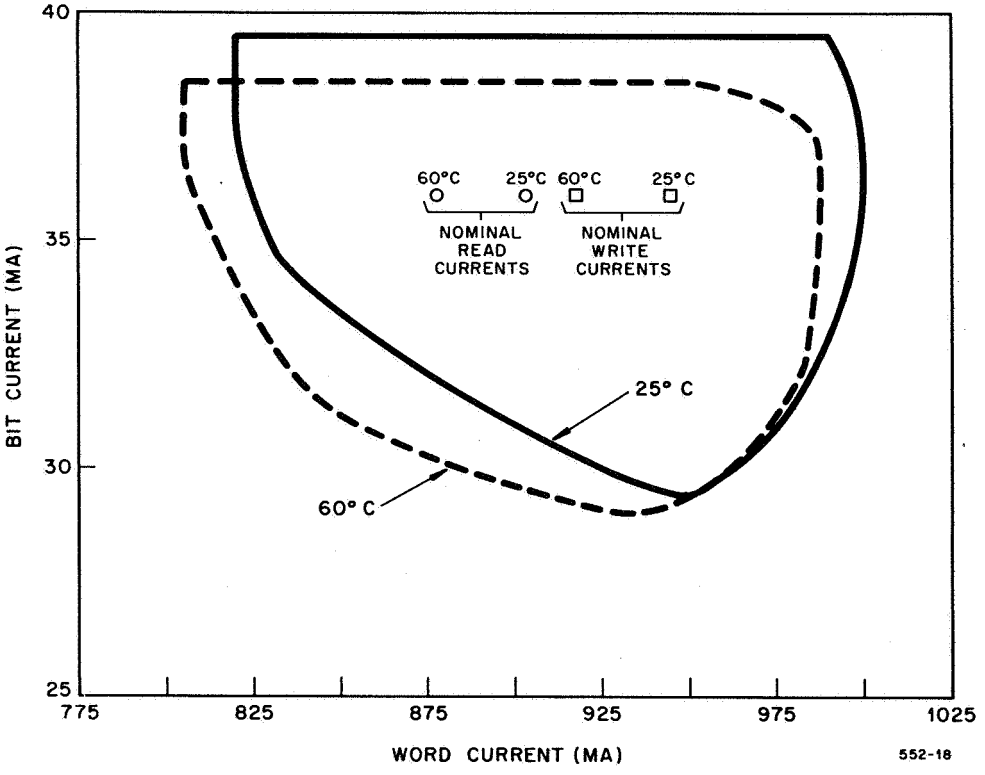


Figure 21. Memory Stack Shmoo

After the system test was completed and the acceptance test performed (Heading 7.4) the worst case information patterns were read 10,000 times without error at nominal currents.

7.3. POWER REQUIREMENT

Figure 22 summarizes the power requirements of the memory. The supply currents for reading and writing were measured at the maximum bit rate of 500 kilocycles. The power requirements for lower bit rates can be obtained by proportionately reducing the difference between the running and standby powers. Although the power levels are higher than specified, the running powers can be met without a significant effort. To reduce the standby power below 500 milliwatts would require a redesign effort.

	Standby		Writing		Reading	
Supply	I-ma	P-mw	I-ma	P-mw	I-ma	P-mw
+24.5	0.0	0	13.6	334	11.5	282
+12.0	12.0	144	60.0	720	63.0	756
+ 6.0	54.0	324	77.0	462	92.0	552
+ 3.0	6.9	21	1.0	3	-9.8	---
- 3.0	30.0	90	27.0	81	16	48
Total		579mw		1600		1638

Figure 22. System Power Requirements

7.4. ACCEPTANCE TEST

The following is the acceptance test which the memory system passed without error prior to delivery:

The testing of the memory system shall be performed using the memory exerciser. Worst case information patterns shall be used in the test plan. The worst case pattern for the memory system occurs when the information alternates between "1" and "0" on each successive bit. The worst case pattern whose first bit is a "0" is defined as the "0" pattern, and the worst case pattern whose first bit is a "1" is defined as the "1" pattern.

Program 1:

a. Write "1" pattern into all storage locations.
b. Write "0" pattern into all storage locations.
c. Read all storage locations 100 times.
d. Write "1" pattern into all storage locations.
e. Read all storage locations 100 times.

Program 2:

a. Write "0" pattern into all storage locations.
b. Read all storage locations 3 times.
c. Write "1" pattern into all storage locations.
d. Read all storage locations 3 times.
e. Repeat (a) through (d) as long as required by steps 3 and 6 of the acceptance test.

The following tests shall be performed in the acceptance test.

Test A:

a. Set all system voltages 5.0% below nominal.
b. Perform Program 1.

Test B:

a. Set all system voltages 5.0% above nominal.
b. Perform Program 1.

Test C:

a. Set all system voltages at nominal.
b. Perform Program 2.

The following is the acceptance test. The information rate shall be 500 kilocycles for all tests.

1. Perform Test A at 25°C.
2. Perform Test B at 25°C.
3. Perform Test C starting at 25°C. and continue to perform Test C while the ambient temperature is being raised to 55°C. at a rate of approximately 1 C. per minute and for 30 minutes after the ambient temperature has reached 55°C.
4. Perform Test A at 55°C.
5. Perform Test B at 55°C.
6. Perform Test C starting at 55°C., and continue to perform Test C while the ambient temperature is being lowered to 25°C. at a rate of approximately 1°C. per minute and for 30 minutes after the ambient temperature has reached 25°C.
7. Perform Test A at 25°C.
8. Perform Test B at 25°C.

The above test plan takes four and one-half hours from start to finish.

APPENDIX I

CIRCUITS AND LOGICS

I.1. LOGIC NOTATION

The logic notation used for the memory logics will be described with reference to the logic blocks shown in Figure I-1 and Figure I-2. These blocks are taken from Drawing 3836145. The same logic notation as described here is also used on the memory exerciser logics in Appendix III.

Within each logic block there are up to five types of information. Figure I-1 contains all five types, whereas Figure I-2 contains only Types 2, 4 and 5. These types are as follows:

Type 1: Logic Function

This type describes the logic function performed in the logic block. In Figure I-1 an "or" function is being performed. Type 1 information is optional since the function may be obvious from the circuit type, as is the case in Figure I-2 where the function of a flip-flop is obvious. The logic functions used in the memory logics are as follows:

Designation	Function
A	AND
OR	OR
N	INVERT

Type 2: Circuit Type

This type gives the circuit type performing the function. In Figure I-1, SS stands for Single Shot and in Figure I-2, FF1B stands for Flip-Flop 1B. A complete cross reference list is given in Section I.3 of the circuit types and circuit schematics on which they appear.

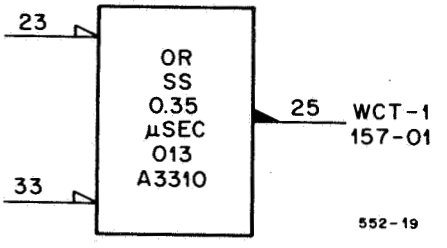


Figure I-1. Single Output Logic Block

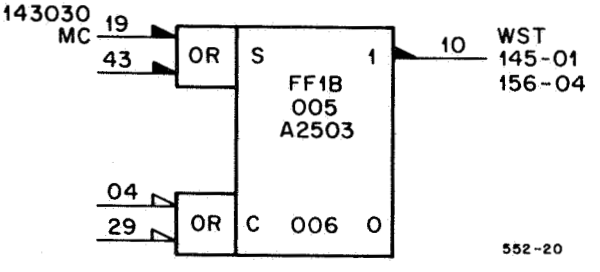


Figure I-2. Dual Output Logic Block

Type 3: Miscellaneous

This type, when used, gives information necessary with certain citcuit types to understand the logics. For example, the time duration of the Single Shot is given in Figure I-1.

Type 4: Component Number

Each single output logic block contains a component number (013 in Figure I-1). The logic blocks on each drawing are sequentially numbered. Each logic block is uniquely identified by first giving the last 3 numbers of the drawing number and then giving the component number. Thus the block in Figure I-1 is identified by 145013. For a block which has more than one output, each output receives a component number so that the output can be uniquely identified at the input which the circuit drives.

Type 5: Component Location and Test Point

The location of each component in the card library is given in each block. In addition, the test point of the output of the component is given if it is available. For example, in Figure I-1, A3310 means the card is in row A, column 33 of the card library and the test point is number 10.

Flags are often used at the inputs and outputs to assist the understanding of the logic function being performed. A light flag indicates a low signal and a dark flag indicates a high signal. The normal logic levels in the memory are ground and +6 volts for the low and high levels respectively. Levels other than this are shown on the logics. The flags at the outputs show the active level of the logic block. The flag on the output in Figure I-1 shows that the output goes positive when the single shot is triggered. The flag on the output in Figure I-2 shows that the output goes positive when the flip-flop is set. The flags at the inputs show the activating levels for the logic block. A negative going input in Figure I-1 will trigger the single shot, a positive going set input in Figure I-2 will set the flip-flop, and a negative going clear input in Figure I-2 will reset the flip-flop.

The numbers adjacent to the input and output flags are the numbers of the wire wrap pins on the backboard of the card library. 25 is the pin number of the output in Figure I-1. An XX where a pin number normally goes indicates on-card wiring.

Signal titles appear where the interconnection of logic blocks do not appear on the drawing. WST is the signal title of the output in Figure I-2. Next to an output signal title is the information which gives the inputs

which the output drives. 145-01 and 156-04 under WST says that WST appears once on the drawing whose last three numbers are 145 and appears four times on the drawing whose last three numbers are 156. MC is the signal title of an input in Figure I-2, and the source of the input is component 143020. A list of the signals and their functions is given in Heading I-2.

Inputs to a logic block which perform different functions are uniquely labeled in the block. The inputs which set the flip-flop in Figure I-2 appear opposite the S, and the inputs which clear the flip-flop appear opposite the C. Logic blocks which have more than one output receives a unique identification in addition to the component numbers. In Figure I-2 the flip-flop outputs are identified by 1 and 0. These input and output identifications are necessary to reference to the circuit schematics.

I.2. SIGNAL LIST

The following is a list of the signal titles used in the memory logics. The list gives the last three numbers of the logic print on which the source of the signal appears.

Signal Title	Signal Source Print	Signal Function
A1 thru A22	157	These are the outputs of the 22 A-switches and are connected to the word line diodes in the memory stack. Only one of the A-switches in activated at a time.
A1-0	159	This indicates the state of the first stage of the A1 ring counter and is used to check synchronization.
A1-1 thru A1-4	156	These are the 1 outputs of the A1 ring counter and drive the A-switch drivers.
$\overline{\text{A1-1}}$ thru $\overline{\text{A1-4}}$	156	These are the 0 outputs of the A1 ring counter
A2-0	159	This indicates the state of the first stage of the A2 ring counter and is used to check synchronization.
A2-1 thru A2-6	156	These are the 0 outputs of the A2 ring counter and are primarily used to select the A switches.

Signal Title	Signal Source Print	Signal Function
BCC		Block Counter Clear: This exerciser signal blocks the clearing of the word counters when one of the block step switches is used on the exerciser.
BB1C		Block B1 Counter: This exerciser signal blocks the stepping of the B1 counter.
BB2C		Block B2 Counter: This exerciser signal blocks the stepping of the B2 (plane) counter.
BPC		Block P Counter: This exerciser signal blocks the stepping of the position counter.
BB2C1	159	This blocks the stepping of the B2 ring counter. This is an exerciser function only.
BC1 and BC4	154	These are the logic signals which indicate the state of the first and fourth stages of the Buffer Counter.
BCR1 thru BCR4	154	These enable information to be gated from the Buffer Register into the Output Flip-Flop in the read cycle.
BCW1 thru BCW4	154	These gate the input data into the Buffer Register. The gate time is controlled by GBR1.
BPP	145	Bit Power Pulse. This steps up the current level of the Information Register during the write cycle.
BRO1 thru BRO4	154	Buffer Register Output. These determine the information to be gated into the Output Flip-Flop in the read cycle and to be gated into the Information Register in the write cycle.
BS	156	Sets the first stage of the B2 ring counter.
BT1 and BT2	145	These are the timing pulses which drive the bit drivers and control the timing of the first and second bit currents.
B1 thru B96	157	These drive the B-switch transistors on the memory planes. Only one of the 96 is activated at a time.
B1-0	159	This indicates the state of the first stage of the B1 ring counter and is used to check synchronization.

Signal Title	Signal Source Print	Signal Function
B1-1 thru B1-4	156	These are the 1 outputs of the B1 ring counter and drive the B switch drivers.
$\overline{\text{B1-1}}$ and $\overline{\text{B1-4}}$	156	These are the 0 outputs of the first and fourth stages of the B1 ring counter.
B1-11 thru B1-14	157	These are the outputs of the B-switch drivers.
B2-0	159	This indicates the state of the first stage of the B2 ring counter and is used to check synchronization.
B2-1 thru B2-24	156	These are the outputs of the B2 ring counter and are primarily used to select the B-switches.
CB1	159	This clears the B1 counter when block step is used.
CBR1CCC	143	This is the timing pulse which clears the buffer register, the converter counter and the information register when the read-write command changes.
CC	156	Common clear: This clears the 2 thru n stages of the five Word Counters.
CCC	154	Converter Counter Clear.
CIR	145	Clear Information Register
CWC	145	Clear Word Counter: This is the timing pulse which clears the word counters when the Read-Write Command changes.
CW1C	159	This is the output of the gate which blocks CWC when the Block Counter Step is being performed by the exercises.
D1-1, D1-2, D2-1, and D2-2	158	These signals drive the dummy bit-sense matrix switches.
END OF READ	143	This is the memory output signal which occurs when the last bit in the memory has been read.
END OF WRITE	143	This is the memory output signal which occurs when the last bit in the memory has been written.
GBRI	143	Gate Buffer Register In: This timing signal is referred to under signals BCW1 thru BCW4.

Signal Title	Signal Source Print	Signal Function
GBRO	143	Gate Buffer Register Out: This timing signal is referred to under signals ICR1 thru ICD9.
GIR	143	Gate Information Register: This timing signal referred to under signals ICW1 thru ICW9.
GOFF	143	Gate Output Flip-Flop: This timing signal controls the time during the read cycle when information is transferred from the Buffer Register to the Output Flip-Flop.
IC1 and IC9	154	These are the logic signals which indicate the state of the first and ninth stages of the Information Counter.
ICC1 thru ICC9	154	0 outputs of Information Counter.
$\overline{\text{ICC1}}$ thru $\overline{\text{ICC9}}$	154	1 outputs of Information Counter which enable the Converter Counter Pulses.
ICR1 thru ICR9	154	These gate information from the Information Register to the Buffer Register during a read cycle. The timing of the signals is controlled by GBRO.
ICW1 thru ICW9	154	These gate information from the Buffer Register to the Information Register in the Write cycle. The timing of the signals is controlled by GIR.
INPUT CLOCK	143	This is the controlling clock to the memory.
INPUT DATA	154	This is the information line to the memory.
IRO1 thru IRO4	155	These are the information signal lines from the Information Register to the Buffer Register. Information is gated into the lines by ICR pulses.
LBR1	145	Load Buffer Register 1: This delays the transfer of the first four bits from the Information Register to the Buffer Register in the Read cycle.
MC	143	Memory Clock: This initiates the 36 bit parallel Read cycle or Write cycle.
Output Clock	143	Output from memory indicating presence of Output Data.
Output Data	145	Information output line of the memory.

Signal Title	Signal Source Print	Signal Function
PS	156	Sets the first stage of the P ring counter.
PST	145	Position Select Timing: This is the timing pulse for selecting the bit-sense matrix.
P-0	159	This indicates the state of the first stage of the P ring counter and is used to check synchronization.
P1 thru P16	156	These are the 1 outputs of the P ring counter and drive the bit-sense matrix drivers.
$\overline{P1}$ and $\overline{P16}$	156	There are the 0 outputs of the first and last stages of the P ring counter.
P1-1 thru P1-16 & P2-1 thru P2-16	158	These drive the plated wire bit-sense matrix swtiches. The timing is controlled by PST.
RAG1 thru RAG4	145	Read Amplifier Gate: These gate the read amplifiers during the read cycle.
R	143	Read: This is the logic signal used to indicate the memory is reading information.
Read-Write Command	143	This is the input signal to the memory which determines whether a read operation or write operation is being performed.
R1	143	Read 1: This signal initiates the first 36 bit parallel read after the read command has been received.
SA1, SA2, SB1	159	This clears the first stages of the A1, A2 and B1 counters when the P or B2 counter is blocked.
SBC	143	Step Buffer Counter: This is the timing signal which controls the stepping of the Buffer Counter.
SIC	154	This is the step pulse for the Information Counter. The Timing is controlled by signal SICCBR.
SICCBR	143	This is the timing signal which controls the stepping of the Information Counter and the clearing of the Buffer Register.
SPC	159	Stop Position Counter: This is an exerciser function which blocks the stepping of the position counter.

Signal Title	Signal Source Print	Signal Function
SWC	145	Step Word Counter: This is the timing signal that advances the B1 counter.
SWIC	159	Signal SWC is gated to enable the exerciser to inhibit the word counter stepping. SWIC drives the B1 step circuit and is inhibited on command from the exerciser.
TB	156	
TP	156	
W	143	Write: This is the logic signal used to indicate the memory is writing information.
WCT1 and WCT2	145	Word Current Timing: These are the timing pulses which determine the duration of the word currents.
WST	145	Word Select Timing: This controls the time during which the A-switches and B-switches are enabled.

I.3. PRINTED CIRCUIT CARD TYPES

The following cross reference list gives the circuit identifiers (Type 2 information in Heading I.1) and the Printed Circuit Card Type on which the circuit schematics are drawn.

Identifier	Circuit Type	Card Type
AS	A-Switch	7
ASD	A-Switch Driver	14
BC-1	Blcok Counter 1	10
BC-2	Block Counter 2	10
BPC	Bit Path Circuit	1
BPP	Bit Power Pulser	4
BRC	Buffer Register Clear	9
BRG	Buffer Register Gate	9, 12
BS	B-Switch	3
BSD	B-Switch Driver	14
BTP	Bit Timing Pulser	4
CB1	Clear B1	19
CC	Converter Counter	13
CCC	Converter Counter Clear	16
CCI	Converter Counter Inverter	12

Identifier	Circuit Type	Card Type
CCP	Converter Counter Pulser	13
CCS	Converter Counter Step	12
CD	Counter Decoder	16, 19
DMD	Dummy Matrix Driver	2
FF1	Special Flip Flops	17, 19, 20
FF2	Output Flip Flop	16
FF3	Buffer Registers	9
IIF	Input Interface	12
IROG	IRO Gate	12
MOI	Output Interface	12
N	Inverter	12
PA	Pulse Amplifier	12
PG	Pulse Gate	11, 20
PG-1	Pulse Gate-1	17
RGP	Read Gate Pulser	5
SS	Delay Flop	11
SS1	Word Counter Delay Flop	14
WC	Word Counter	8
WCB	Word Counter Bypass	14
WCC	Word Counter Clear	4
WCD	Word Counter Driver	6
WCO	Word Counter Output	10
WCR	Word Current Regulator	18
WCS	Word Counter Stepper	6
WMD	Wire Matrix Driver	2
WSR	Write Step Regulator	18

I.4 LOGIC AND CIRCUIT SCHEMATICS

The detailed logics and circuit schematics of the memory system are contained in a separate folder and can be obtained from the GSFC Technical Officer/code 731. A list of the drawings available is given in front matter of this report.

APPENDIX II

MECHANICAL DRAWINGS

This appendix contains the mechanical assembly drawings of the memory frames. These drawings are contained in a separate folder and can be obtained from the GSFC Technical Officer/Code 731. A list of the drawings available is given in the front matter of this report.

APPENDIX III

MEMORY EXERCISER OPERATING INSTRUCTIONS

The function of the memory exerciser is to provide information patterns for the memory to write and to check contents of the memory when it is read out. The memory exerciser basically contains counters which duplicate the memory counters, an information generator which is a function of the count, and logic which compares the contents of the memory and the exerciser. If the contents do not compare, an error is indicated. The exerciser also contains a cycle counter. In normal operation the selected information pattern will be written into the memory and then read three times. The exerciser can also be operated in a continuous write or continuous read mode. In addition to providing information patterns to the memory, the exerciser supplies the memory with the read-write command and the input clock. The frequency of operation is controlled by an external generator. In addition to checking information, the exerciser checks the memory word counters, to assure the two units are in synchronization, and the output clock. The operation of the exerciser will now be explained by describing the functions of the individual switches.

POWER ON AND POWER OFF

The exerciser contains its own power supplies.

These switches turn the exerciser supplies on and off.

CLEAR

Prior to starting a test the exerciser and memory must be cleared to establish initial synchronization. This is done by first depressing the test switch and then the memory switch.

START AND STOP

These switches are used to start and stop the exerciser.

COMPLEMENT

B. When this switch is in the down position, opposite information will be written in adjacent bits on the plated wires.

PO When this switch is in the down position, opposite information will be written in adjacent plated wires.

Alt. 1-0 When this switch is in the down position and the exerciser is operating in the normal write-three read mode, the information in the memory will be complemented on each write cycle.

ITS Only used when system being built.

BIT SWITCHES

These switches are used to write different information in the parallel bits of the memory. Each switch controls bit n and bit n + 20, where n is the number of the switch. With the complement switches off, the information will be as indicated by the switches.

ADDRESS LIGHTS

The address is indicated by the address lights of the five address counters. These counters are the I (information), B, A, PO (position) and PL (plane) counters. The state of a particular counter is the sum of the lights of that counter. The I counter indicates which of the 36 parallel bits is being addressed and the B, A, PO, and PL counters give the word address. During the write mode the lights indicate the address of the next bit to be read out, and the word counter gives the address of the next word to be read out. The cycle lights indidate whether the memory is being exercised in the write mode or the read mode and whether the memory is being read for the first, second, or third time in normal operation.

I SWITCHES AND PBI

During the debugging of the memory, it was often desirable to test only one of the 36 parallel bits for information errors. To do this, the PBI switch is depressed and the desired bit is determined by the sum of the I switches which are depressed.

WORD SWITCHES AND PSWI

During the debugging of the memory, it was often desirable to stop at a particular word address. To do this, the PSWI switch was depressed and the desired address selected by depressing the appropriate word switches. The desired address of each counter is determined by the sum of the switches depressed for each counter. The exerciser would stop when it cycles up to the desired address. The exerciser will

stop during the write cycle if neither cycle switch is depressed, during the first read if the left cycle switch is depressed, during the second cycle if the right cycle switch is depressed, and during the third read if both cycle switches are depressed.

READ-WRITE SWITCH (RWSW)

This three-position switch selects the continuous write mode, the continuous read mode, or the normal write-three read mode of operation. Note: To switch to continuous write the exerciser must be in the write mode, and to switch to continuous read the exerciser must be in a read mode.

ERROR OVERRIDE

If an error of any type occurs, the exerciser will normally stop at the address indicated by the lights. When the error override switch is depressed, however, the error lights will come on, but the exerciser will continue running.

ERROR LIGHTS

These lights indicate the type of error which occurred. The exerciser checks the memory information, the first stage of each word counter in the memory, and the memory output clock (MIC).

EFCL

This switch is used to manually clear the error flip-flop which becomes set when an information error occurs. Depressing this switch thereby causes the bit error light to go out after a bit error has occurred.

PMRW

This switch was used only when the system was being built.

BC STEP (Block Counter Step)

During the debugging of the memory it was often desirable to cycle through only part of the memory. This was accomplished with the Block Counter Step switches. If it is desired to cycle through only one of the 24 memory planes, the exerciser would be cycled up to the desired plane and stopped (using PSWI), the PL switch depressed, PSWI removed, and the exerciser then started again. Similarly, a particular position on a plane is cycled by depressing the PO switch after the desired addressed is reached. Any word address can be cycled by depressing the B switch after the desired address is reached. Note: The block B and complement B functions cannot be used simultaneously, and the block PO and complement PO cannot be used simultaneously.

GENERATOR INPUT

An external generator must be connected to the exerciser. The generator cable is attached to the card library inside the back of the cabinet.

The exerciser requires a negative pulse going from ground to -8 volts. The pulse width is 350 μs, and the frequency anything up to 500 kilocycles.

The memory is operated with the exerciser by plugging the exerciser cable into the memory, by supplying +24.5 volts and -3.0 volts to the memory, and by performing the functions described above.

The exerciser logic prints are contained in a separate folder and can be obtained from the GSFS Technical Officer/code 731. A list of the drawings available is given in the front matter of this report.